Reg. No. | | | | | | | | | | | | |

Question Paper Code : 57281

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Third Semester

Electronics and Communication Engineering

EC 6302 – DIGITAL ELECTRONICS

(Common to Mechatronics Engineering and Robotics and Automation Engineering)

(Regulations 2013)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. Prove the Boolean theorems : (a) $x + x = x$

   (b) $x + xy = x$

2. Define Noise margin.

3. Write the design procedure of combinational circuit.

4. Draw the combinational circuit that converts 2 coded inputs into 4 coded outputs.

5. Differentiate synchronous and asynchronous sequential circuits.

6. Give the truth table of transparent latch.

7. Give the classification of programmable logic devices.

8. How the bipolar RAM cell is different from MOSFET RAM cell ?

9. What is Hazard ? Give its types.

10. Define critical race and give the methods for critical-race free state assignment.

PART – B (5 × 16 = 80 marks)

11. (a) Simplify the following Boolean function F, using Quine Mccluskey method and verify the result using K-map F(A, B, C, D) = Σ (0, 2, 3, 5, 7, 9, 11, 13, 14) **(16)**

OR

(b) (i) Draw and explain Tri-state TTL inverter circuit diagram with its operation. **(10)**

(ii) Implement the following function using NAND and inverter gates. **(6)**

F = AB + A'B' + B'C

12. (a) (i) Design a 4-bit magnitude comparator with 3 outputs : A > B, A = B, A < B. **(8)**

(ii) Design a 4 bit binary to gray code converter. **(8)**

OR

(b) (i) Implement the following Boolean function using 8 × 1 Multiplexers.

F (A, B, C, D) = Σ (1, 3, 4, 11, 12, 13, 14, 15) **(8)**

(ii) Explain the concept of carry look ahead adder with neat logic diagram. **(8)**

13. (a) Design a 3-bit synchronous counter using D-flip flop. **(16)**

OR

(b) (i) Draw and explain the 4-bit SISO, SIPO, PISO and PIPO shift register with its waveforms. **(12)**

(ii) Realize D flip-flop using SR flip-flop. **(4)**

14. (a) (i) Implement the following function using PLA. **(12)**

F1 $(x, y, z) = \Sigma m (1, 2, 4, 6)$

F2 $(x, y, z) = \Sigma m (0, 1, 6, 7)$

F3 $(x, y, z) = \Sigma m (2, 6)$

(ii) Write short notes on FPGA. **(4)**

OR

(b) (i) Explain memory READ and WRITE operation with neat timing diagram. **(8)**

(ii) Explain the organization of ROM with relevant diagrams. **(8)**

15. (a) Design an asynchronous sequential circuit with two inputs X_1 and X_2 and with one output Z. When X_1 is 0, the output Z is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0. **(16)**

OR

(b) Construct the transition table, state table and state diagram for the more sequential circuit given below. **(16)**